REMARKS/ARGUMENTS

Claims 1-6 are pending in the present application. Claims 1 and 5 have been amended. Reconsideration and allowance of claims 1-6 of the present application are respectfully requested.

Oath/Declaration

The Office Action requested a new oath or declaration because the applicant's citizenship country listed in the oath/declaration is Belguim and in the Application Data Sheet is listed as US. Attached is a Supplemental Application Data Sheet, which corrects the applicant's citizenship in Application Data Sheet to indicate Belguim.

Objection of Specification

The Office Action objected to the Specification of the present application. Specifically, the Office Action stated that the phrase "include and interface element" of the Abstract and the phrase "connection an external tester" on page 4, line 17 are incorrect. As shown, the Abstract has been amended to recite "include an interface element" and page 4, line 17 has been amended to recite "connection with an external tester." Withdrawal of the objection of specification is respectfully requested.

Objection of Claim 5

The Office Action objected to claim 5 because the phrase "connection an external" is incorrect. As shown, claim 5 has been amended to recite "connection with an external." Withdrawal of the objection of claim 5 is respectfully requested.

Section 112, Second Paragraph Rejection of Claim 1

The Office Action rejected claim 1 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner stated that the phrase "absence of positive action" is unclear. As shown, claim 1 has been amended to recite ". . . wherein if the external test circuitry is free from maintaining the integrated circuit in a test mode for a

predetermined period, . . ." Support for the amendment can be found, for example, at page 3, lines 1-4. No new matter is added. Withdrawal of the Section 112, second paragraph, rejection is respectfully requested.

Section 103 Rejection of Claims 1-6

The Office Action rejected claims 1, 2, and 5 under 35 U.S.C. § 103(a) as being unpatentable over JP 57-133656 to Toyofuku et al. ("Toyofuku") in view of U.S. Pat. No. 4,874,610 to Ozawa et al. ("Ozawa"). The Office Action conceded that Toyofuku fails to explicitly teach specifically that in the absence of positive action from the external test circuitry that the integrated circuit defaults from test mode to normal mode. However, the Office Action stated that Ozawa is an analogous art and that it would be obvious to one of ordinary skill in the art at the time the invention was made to modify Toyofuku's patent application with the teachings of Ozawa to achieve the integrated circuit of claim 1.

Applicant asserts that one of ordinary skill in the art would not have been motivated by Ozawa to modify Toyofuku's integrated circuit because Ozawa is not analogous prior art. M.P.E.P. 2141.01(a) I provides that the examiner must determine what is "analogous prior art" for the purpose of analyzing the obviousness of the subject matter at issue. "Under the correct analysis, any need or problem known in the field of endeavor at the time of the invention and addressed by the patent [or application at issue] can provide a reason for combining the elements in the manner claimed." *KSR International Co. v. Teleflex Inc.*, 550 U.S., 127 S. Ct. 1727, 1742, 82 USPQ2d 1385, 1397 (2007).

The integrated circuit of claim 1 includes an interface element allowing the testing of an integrated circuit via a single pin as set forth in Field of the Invention. Unlike the claimed integrated circuit, Ozawa is directed to a method of restoring a dual transmission line which connects respective stations to make a local-area network. (Field of the Invention). Certainly, information transmissions within a local-area network and integrated circuits are unrelated fields. This is evidenced by the assignment of this application to Art Unit 2117, which includes U.S. classification 324/76.47. None of Ozawa's classifications is included in this assigned Unit.

Applicant, therefore, asserts that Ozawa does not relate to the field of the integrated circuit of claim 1.

Further, the nature of the problem to be solved by the claimed integrated circuit is the use of a large number of pins on an integrated circuit. Nothing in the description or drawings of Ozawa is (or considerably can be) directed to such a problem. Indeed, Ozawa's disclosure is directed to a concern of a method of restoring a transmission line which is unable to correct an information transmission fault without carrier breakdown. (Col. 2, lines 49-54). Nothing in the disclosure of Ozawa directs those in the art how to reduce the number of pins on an integrated circuit for testing. Therefore, the disclosure of Ozawa is not reasonably pertinent to the problem to be solved by Applicant's invention. Applicant asserts that the problem solved by Ozawa does not provide a reason for combining the elements of Toyofuku and Ozawa in the manner claimed.

Since Ozawa is not in the same field of the invention and is not reasonably pertinent to the nature of the problem to be solved by the apparatus of claim 1, Applicant asserts that Ozawa is not analogous art upon which the rejection can be made.

Notwithstanding the foregoing, claim 1 has been amended to recite that if the external test circuitry is free from maintaining the integrated circuit in a test mode for a predetermined period, the integrated circuit defaults from the test mode to a normal mode. Applicant further asserts that the combination of Toyofuku and Ozawa fail to disclose the claimed feature as shown above.

As conceded by the Office Action, Toyofuku fails to teach that in the absence of positive action from the external test circuitry that the integrated circuit defaults from test mode to normal mode. Applicant submits that Toyofuku fails to disclose the amended feature that if the external test circuitry is free from maintaining the integrated circuit in a test mode for a predetermined period, the integrated circuit defaults from the test mode to a normal mode.

As argued above, Ozawa is directed to a method of restoring a dual transmission line which connects respective stations to make a local-area network. The problem described in Ozawa is not related to that to be solved by the integrated circuit of claim 1. Furthermore, col. 6, lines 27-31 of Ozawa is shown below:

> Since the test frame is unable to reach the downstream station S2 because of the information transmission fault, the station S1 experiences a time-out in the test mode 1 and forms a WRAPB state, going to the normal mode M1.

Clearly, nothing in the paragraph shows an external circuitry and an integrated circuit. Further, the paragraph fails to show or even suggest that if the external test circuitry is free from maintaining the integrated circuit in a test mode for a predetermined period, the integrated circuit defaults from the test mode to a normal mode.

Since Toyofuku and Ozawa fail to teach or suggest all elements recited in the amended claim 1, Applicant asserts that claim 1 is not obvious over the combination of these cited references and is, therefore, allowable for at least these reasons set forth above.

Claims 2 and 5 depend from claim 1 and are, therefore, allowable over the art of record by virtue of their dependencies.

The Office Action rejected claim 3 under 35 U.S.C. § 103(a) as being unpatentable over Toyofuku in view of Ozawa and further in view of U.S. Pat. No. 4,947,357 to Stewart et al. ("Stewart"), claim 4 as being unpatentable over Toyofuku in view of Ozawa and further in view of U.S. Pat. No. 4,449,065 to Davies, Jr. ("Davies, Jr."), and claim 6 as being unpatentable over Toyofuku in view of Ozawa and further in view of U.S. Pat. No. 5,404,304 to Wise et al. ("Wise").

Claims 3, 4, and 6 depend from claim 1. Though describing various features, Stewart, Davies, Jr., and Wise fail to cure the deficiency of Toyofuku and Ozawa. That is, Stewart, Davies, Jr., and Wise also fail to disclose that if the external test circuitry is free from maintaining the integrated circuit in a test mode for a predetermined period, the integrated circuit defaults from the test mode to a normal mode. Applicant asserts that claims 3, 4, and 6 are allowable over the art of record by virtue of their dependencies.

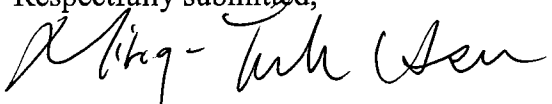
Based on the foregoing, reconsideration and withdrawal of the rejection of claims 1-6 are respectfully requested.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 326-2400.

Respectfully submitted,



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